

INSULATED LOGIC LEVEL TRIAC

<p style="text-align: center; font-weight: bold; font-size: 1.2em;">INSULATED TO-220AB</p> <div style="text-align: center; margin-top: 20px;"> </div> <div style="text-align: center; margin-top: 20px;"> </div>	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border-right: 1px solid black; padding: 5px;"> <p>On-State Current 12 Amp</p> </td> <td style="width: 50%; padding: 5px;"> <p>Gate Trigger Current $\leq 10 \text{ mA}$ (08, 09) $\leq 5 \text{ mA}$ (04)</p> </td> </tr> <tr> <td colspan="2" style="text-align: center; padding: 5px;"> <p>Off-State Voltage 400 V ÷ 800 V</p> </td> </tr> </table> <p>FEATURES</p> <ul style="list-style-type: none"> Glass/passivated die junctions Provides voltage insulated tab (rated at 2500V RMS) Medium current Triac Low thermal resistance High surge current capability Low forward voltage drop Solder dip 260°C, 10s Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C Certified compliance of UL 1557 Standard for Electrically Isolated Semiconductors. Fille reference E320541, Vol. 3 <p style="text-align: right; margin-right: 20px;"> RoHS COMPLIANT </p> <p>MECHANICAL DATA</p> <ul style="list-style-type: none"> Case: INSULATED TO-220AB. Epoxy meets UL 94V-0 flammability rating. Polarity: As marked on the body. Terminals: Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test. <p>TYPICAL APPLICATIONS</p> <p>Logic level versions are designed to interface directly with low power drivers such as microcontrollers.</p>	<p>On-State Current 12 Amp</p>	<p>Gate Trigger Current $\leq 10 \text{ mA}$ (08, 09) $\leq 5 \text{ mA}$ (04)</p>	<p>Off-State Voltage 400 V ÷ 800 V</p>	
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<p>Off-State Voltage 400 V ÷ 800 V</p>					

Maximum Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 90 \text{ }^\circ\text{C}$	12	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz ($t = 16.7 \text{ ms}$)	125	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz ($t = 20 \text{ ms}$)	120	A
I^2t	Fusing Current	$t_p = 10 \text{ ms}$, Half Cycle	72	A^2s
I_{GM}	Peak Gate Current	20 μs max. $T_j = 125 \text{ }^\circ\text{C}$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125 \text{ }^\circ\text{C}$	1	W
di/dt	Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ns}$ $f = 120 \text{ Hz}$, $T_j = 125 \text{ }^\circ\text{C}$	50	$\text{A}/\mu\text{s}$
T_j	Operating Temperature		(-40 +125)	$^\circ\text{C}$
T_{stg}	Storage Temperature		(-40 +125)	$^\circ\text{C}$
T_{sld}	Soldering Temperature	10s max	260	$^\circ\text{C}$
V_{iso}	R.M.S. isolation voltage 50/60 Hz sinusoidal waveform		2.500	Vac

SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	400	600	800	V

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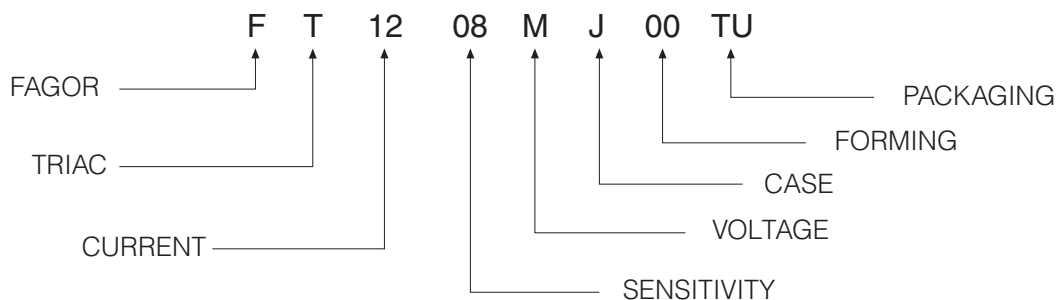
Electrical Characteristics at Tamb = 25 °C

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY			Unit
					04	08	09	
I _{GT} ⁽¹⁾	Gate Trigger Current	V _D = 12 V _{DC} , R _L = 33Ω, T _j = 25 °C	Q1÷Q3	MAX	5	10	10	mA
			Q4	MAX	-	-	10	mA
V _{GT}	Gate Trigger Voltage	V _D = 12 V _{DC} , R _L = 33Ω, T _j = 25 °C	Q1÷Q3	MAX	1.3	1.3	-	V
			Q1÷Q4	MAX	-	-	1.3	V
V _{GD}	Gate Non Trigger Voltage	V _D = V _{DRM} , R _L = 3.3 KΩ, T _j = 125 °C	Q1÷Q3	MIN	0.2	0.2	-	V
			Q1÷Q4	MIN	-	-	0.2	V
I _H ⁽²⁾	Holding Current	I _T = 100 mA, Gate open, T _j = 25 °C		MAX	15		20	mA
I _L	Latching Current	I _G = 1.2 I _{GT} , T _j = 25 °C	Q1,Q3	MAX	10	25	-	mA
			Q1,Q3,Q4	MAX	-	-	20	mA
			Q2	MAX	20	30	25	mA
dV/dt ⁽²⁾	Critical Rate of Voltage Rise	V _D = 0.67 x V _{DRM} , Gate open T _j = 125 °C		MIN	20	40	50	V/μs
(dI/dt) _c ⁽²⁾	Critical Rate of Current Rise	(dv/dt) _c = 0.1 V/μs T _j = 125 °C		MIN	3.5	6.5	2.5	A/ms
		(dv/dt) _c = 10 V/μs T _j = 125 °C		MIN	1	2.9	1.5	A/ms
V _{TM} ⁽²⁾	On-state Voltage	I _T = 17 Amp, t _p = 380 μs, T _j = 25 °C		MAX	1.55			V
V _{t(o)} ⁽²⁾	Threshold Voltage	T _j = 125 °C		MAX	0.85			V
r _d ⁽²⁾	Dynamic resistance	T _j = 125 °C		MAX	35			mΩ
I _{DRM} /I _{RRM}	Off-State Leakage Current	V _D = V _{DRM} , T _j = 125 °C		MAX	1			mA
		V _R = V _{RRM} , T _j = 25 °C		MAX	5			μA
R _{th(j-c)}	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.3			°C/W
R _{th(j-a)}	Thermal Resistance Junction-Ambient				60			°C/W

(1) Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

Part Number Information



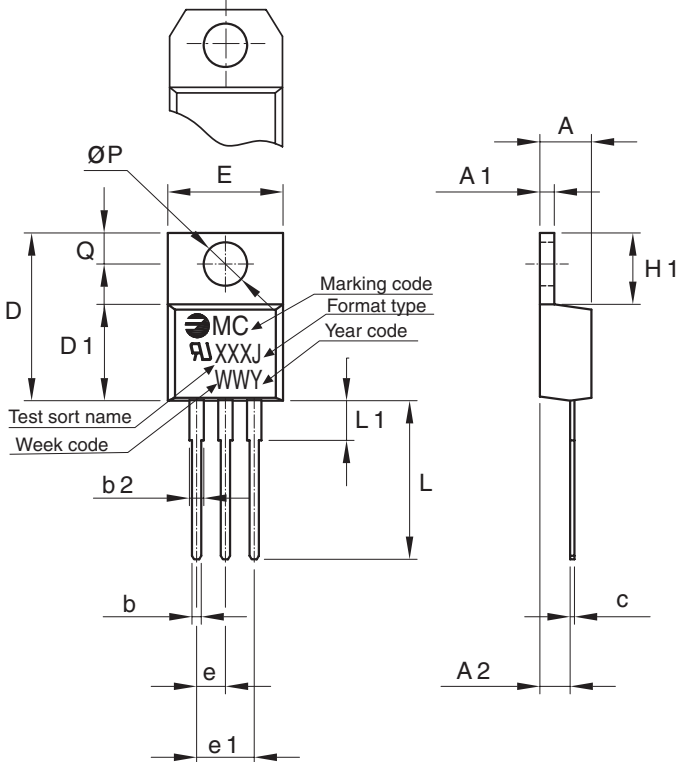
INSULATED LOGIC LEVEL TRIAC

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT1208MJ 00TU	TU	TUBE	1000	2.30

Package Outline Dimensions: (mm) INSULATED TO-220AB

Optional with chamfer



The drawing shows a top view and a side view of the package. The top view includes dimensions: $\varnothing P$, E, Q, D, D1, b2, b, e, e1, L, and L1. The side view includes dimensions: A, A1, A2, H1, and c. Marking details include: MC, XXXJ, WYY, Test sort name, Week code, Marking code, Format type, and Year code.

REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	4.40	4.60
A1	1.21	1.32
A2	2.40	2.72
b	0.61	0.88
b2	1.14	1.70
c	0.46	0.70
D	15.15	16.65
D1	8.60	9.70
E	9.80	10.40
e	2.50	2.60
e1	5.00	5.20
H1	6.35	6.95
L	12.85	13.55
L1	3.50	3.80
P	3.70	3.85
Q	2.65	2.95

Mounting Torque	0.8 N.m
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Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

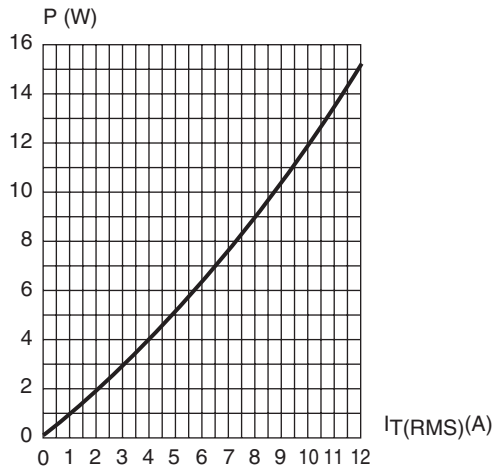


Fig. 2: RMS on-state current versus case temperature (full cycle).

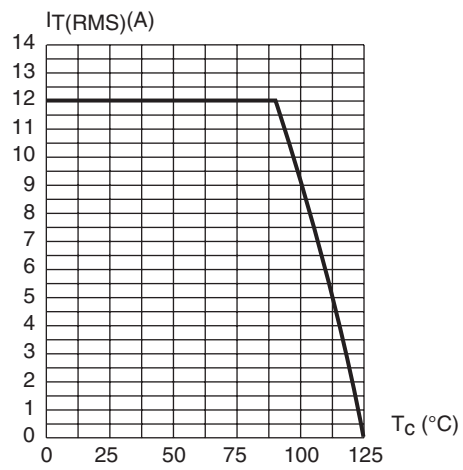


Fig. 3: Relative variation of thermal impedance versus pulse duration.

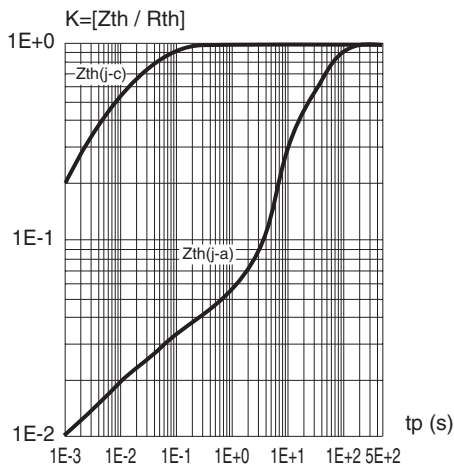


Fig. 4: On-state characteristics (maximum values)

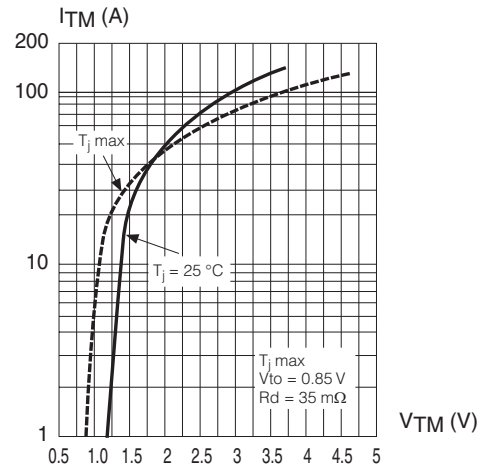


Fig. 5: Surge peak on-state current versus number of cycles

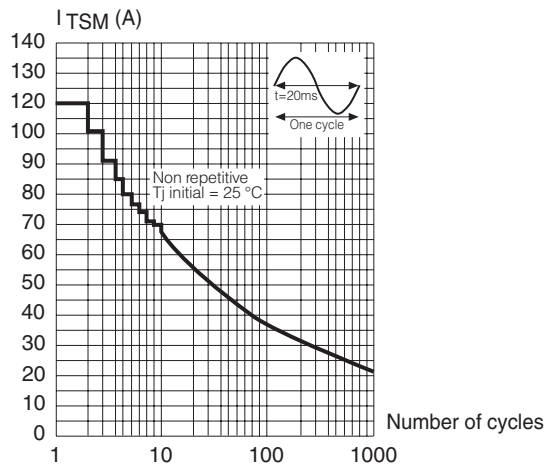
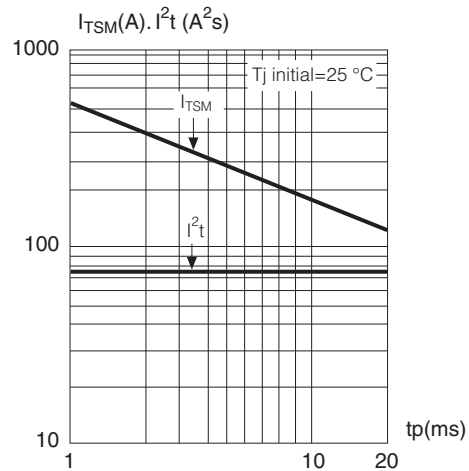


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 20 ms, and corresponding value of I²t.



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Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

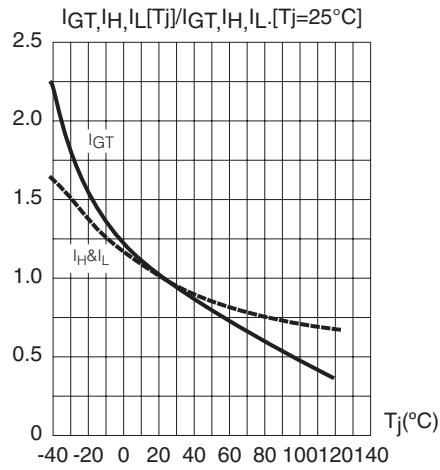


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

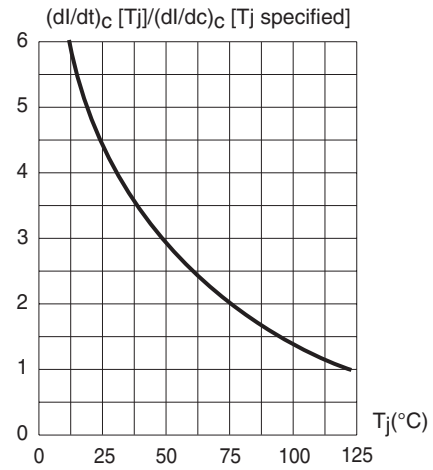
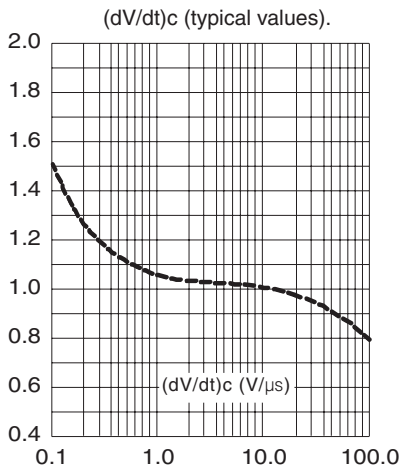


Fig. 9: Relative variation of critical rate of decrease of main current versus



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Revision History

Date	Revision	Description of Changes
14-Oct-2012	0	Original Data Sheet
28-May-2015	1	Change values of Package Outline Dimensions
15-Jun-2016	2	The 09 Sensitivity group introduced
7-Jul-2016	3	I_{L2} modified for 04 Group
28-Aug-2017	4	200V eliminated.

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