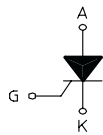
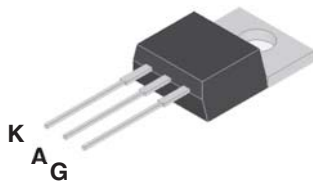


INSULATED STANDARD SCR

INSULATED TO-220AB



On-State Current **Gate Trigger Current**
 25 Amp 2 mA to 40 mA

Off-State Voltage
 200 V ÷ 800 V

These series of **Silicon Controlled Rectifier** use a high performance PNP technology.

These parts are intended for general purpose applications where high gate sensitivity is required. The FS...J series provides an isolated tab (rated at 2500 Vrms).

- * Low thermal resistance with clip bounding
- * Low thermal resistance isolation ceramic for FS...J

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, $T_c = 110\text{ °C}$	25	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, $\Theta = 180\text{ °}$, $T_c = 110\text{ °C}$	16	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	270	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz	250	A
I^2t	Fusing Current	$t_p = 10\text{ms}$, Half Cycle	313	A ² s
I_{GM}	Peak Gate Current	20 μs max.	4	A
P_{GM}	Peak Gate Dissipation	20 μs max.	10	W
$P_{G(AV)}$	Gate Dissipation	20ms max.	1	W
T_j	Operating Temperature		(-40 to +125)	°C
T_{stg}	Storage Temperature		(-40 to +150)	°C
T_{sld}	Soldering Temperature	10s max.	260	°C
V_{RGM}	Reverse Gate Voltage		5	V

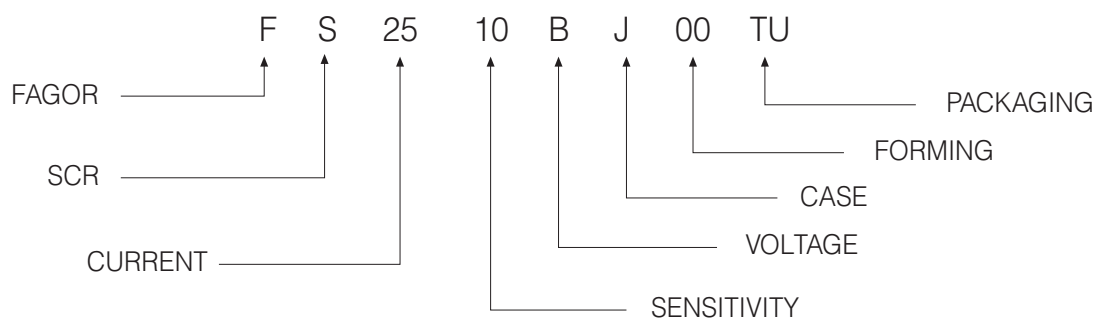
SYMBOL	PARAMETER	CONDITIONS	VOLTAGE					Unit
			B	D	M	S	N	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	$R_{GK} = 1\text{ k}\Omega$	200	400	600	700	800	V

INSULATED STANDARD SCR

Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	SENSITIVITY		Uni	
			10	14		
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 33\Omega, T_j = 25^\circ C$	MIN MAX	2 25	4 40	m A
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 33\Omega, T_j = 25^\circ C$	MAX	1.3		V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3k\Omega, R_{GK} = 220\Omega, T_j = 125^\circ C$	MIN	0.2		V
I_H	Holding Current	$I_T = 500 \text{ mA}$	MAX	40	50	mA
I_L	Latching Current	$I_G = 1.2 I_{GT}$	MAX	60	90	mA
dV / dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, \text{ Gate open}, T_j = 125^\circ C$	MIN	500	1000	V/ μ s
dI / dt	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}, Tr \leq 100 \text{ ns}, f = 60 \text{ Hz}, T_j = 125^\circ C$	MIN	50	100	A/ μ s
V_{TM}	On-state Voltage	at $I_T = 50 \text{ Amp}, tp = 380 \mu\text{s}, T_j = 25^\circ C$	MAX	1.6		V
V_{t0}	Threshold Voltage	$T_j = 125^\circ C$	MAX	0.75		V
r_d	Dynamic resistance	$T_j = 125^\circ C$	MAX	14		m Ω
I_{DRM} / I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}, R_{GK} = 1k\Omega, V_R = V_{RRM}, T_j = 125^\circ C$ $T_j = 25^\circ C$	MAX	2		mA
			MAX	5		μ A
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC	for AC 360° conduction angle		1		°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC	$S = 1 \text{ cm}^2$		60		°C/W

PART NUMBER INFORMATION



INSULATED STANDARD SCR

Fig. 1: Maximum average power dissipation versus average on-state current.

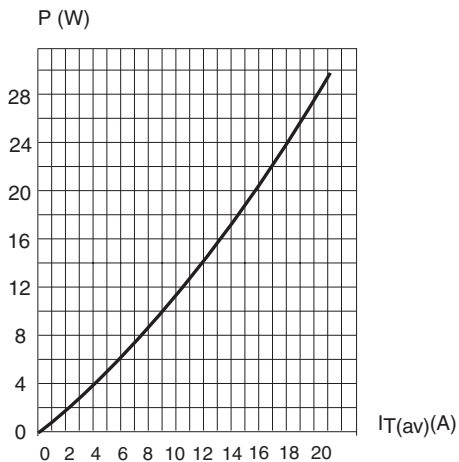


Fig. 2: Average and D.C. on-state current versus case temperature.

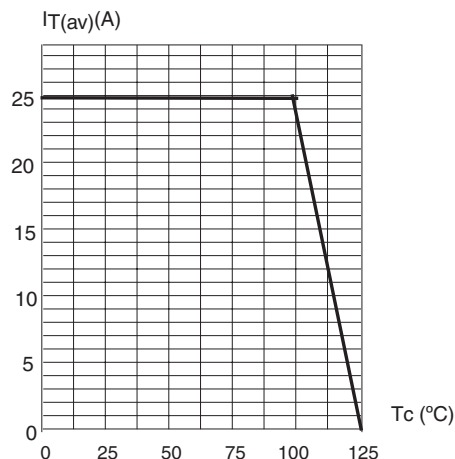


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration.

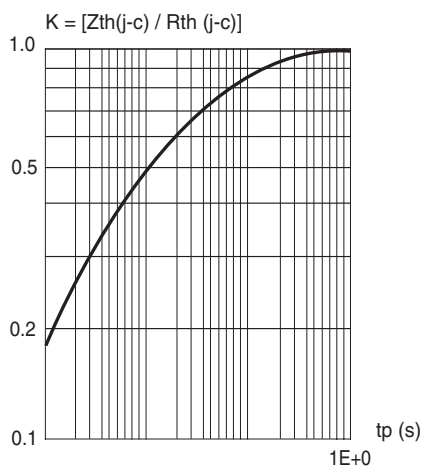


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature.

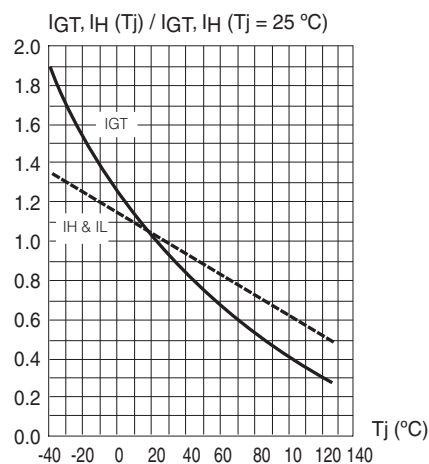


Fig. 5: Non repetitive surge peak on-state current versus number of cycles.

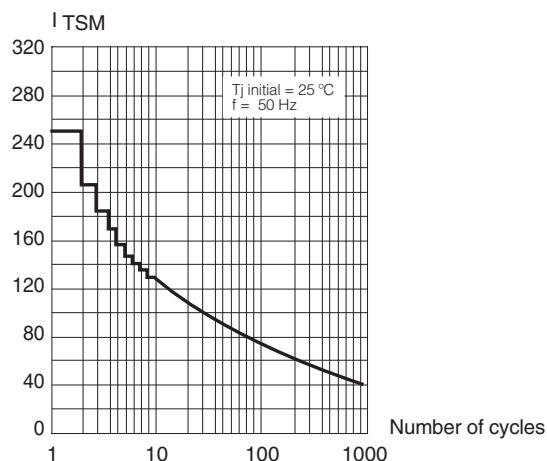
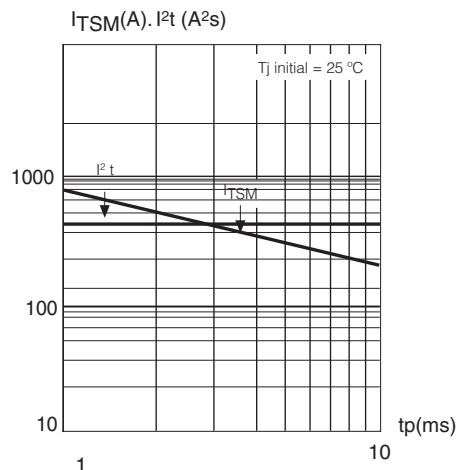
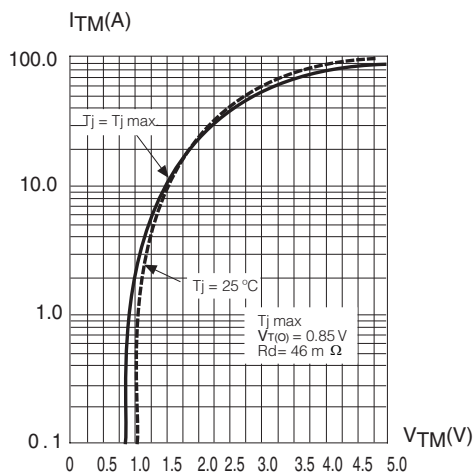


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10$ ms, and corresponding value of I^2t .



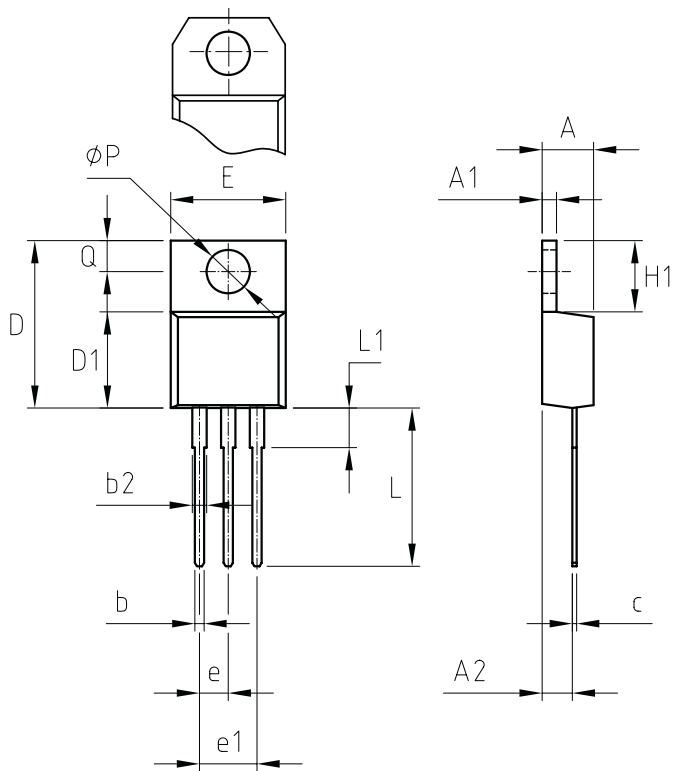
INSULATED STANDARD SCR

Fig. 7: On-state characteristics (maximum values).



PACKAGE MECHANICAL DATA: INSULATED TO-220AB

Optional with chamfer



REF.	DIMENSIONS	
	Milimeters	
	Min.	Max.
A	4.32	4.62
A1	1.21	1.29
A2	2.40	2.70
b	0.80	0.83
b2	1.40	--
c	0.42	0.48
D	15.5	15.68
D1	9.26	9.42
E	10.08	10.24
e	2.54	2.54
e1	5.08	5.08
H1	6.24	6.26
L	12.81	13.81
L1	3.28	4.17
P	3.70	3.80
Q	2.75	2.85

Mounting Torque

1 N.m

(*) Limiting values and life support applications, see Web page.